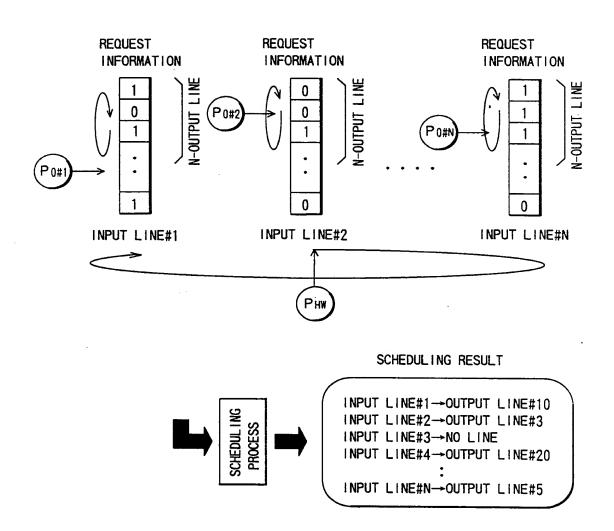
FIG.1



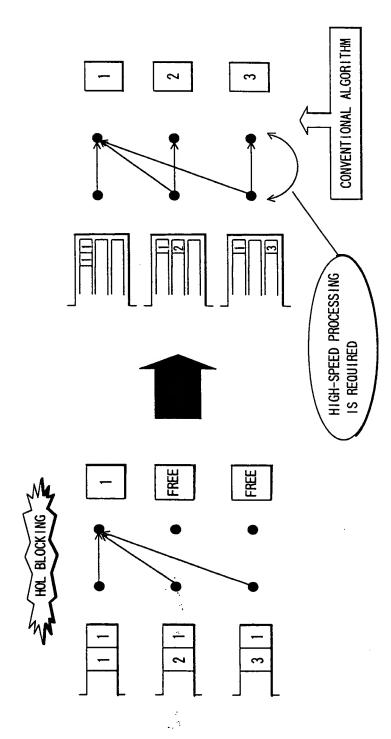
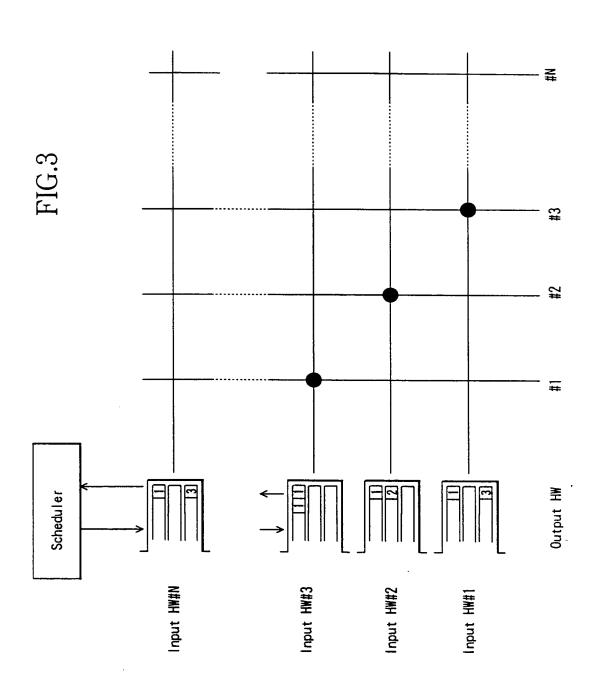
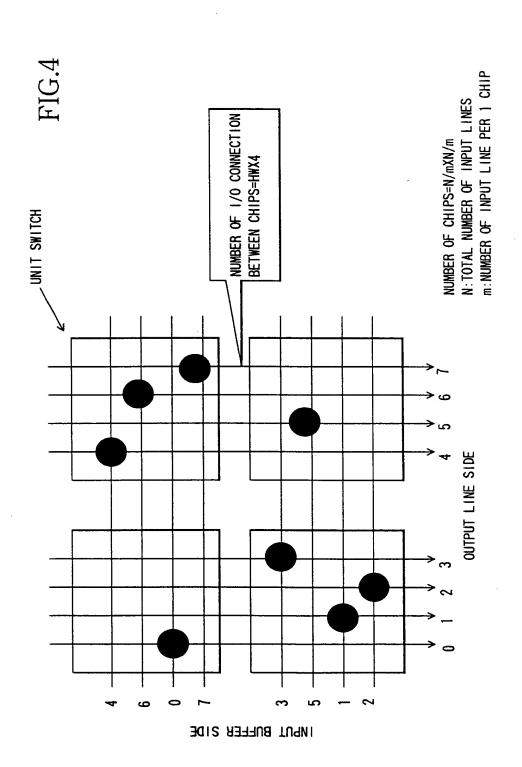
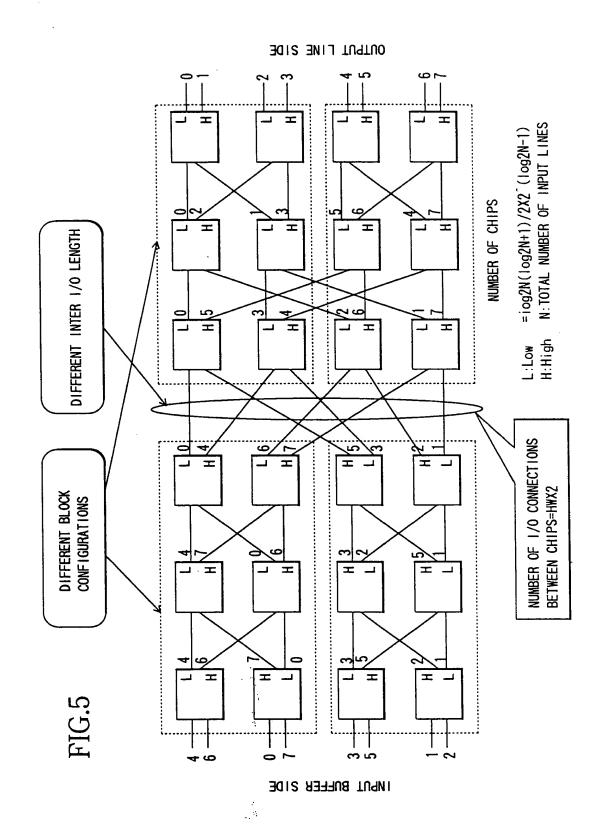
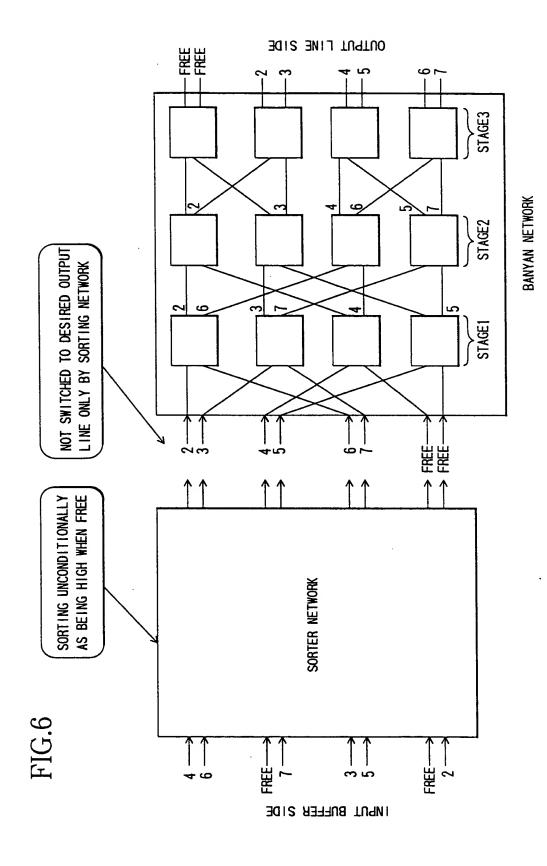


FIG. 2









CELL DATA

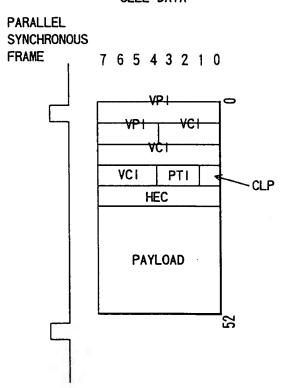
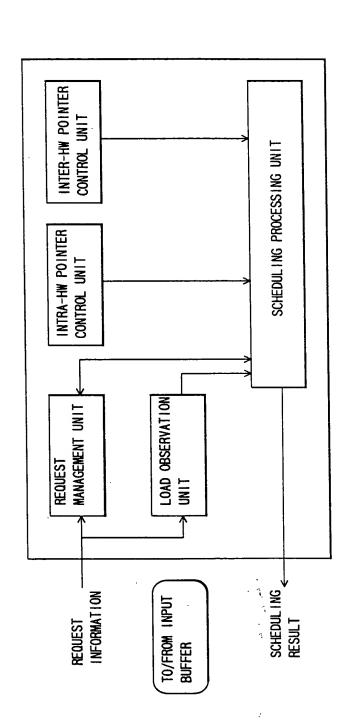
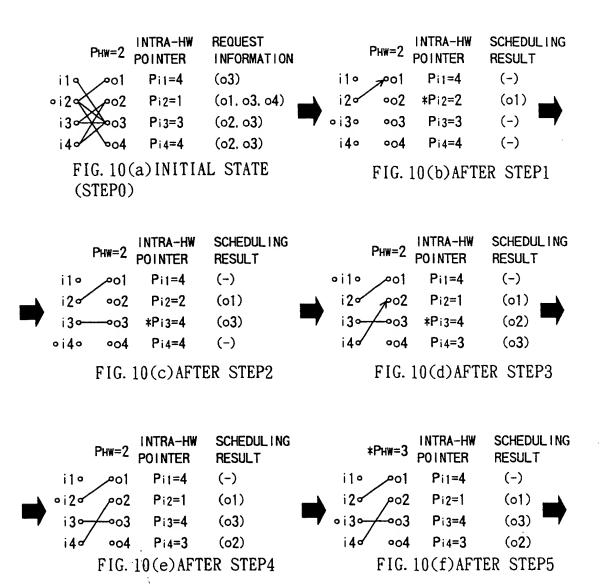


FIG.8



		PHW=1 001 002 003 004 IG. 9(8 STEP0)	INTRA-HW POINTER Pi1=1 Pi2=2 Pi3=3 Pi4=4 a) INITIAL	REQUEST INFORMATION (o3) (o1, o3, o4) (o2, o3) (o2, o3) STATE	→	i1	PHW=1 001 002 003 004 FIG.	INTRA-HW POINTER *Pi1=4 Pi2=2 Pi3=3 Pi4=4	SCHEDULING RESULT (03) (-) (-) (-) R STEP1	
→	i1 q i2 q •i3 • i4 •	PHW=1 ••1 ••2 ••3 ••4 FIG.	INTRA-HW POINTER Pi1=4 *Pi2=1 Pi3=3 Pi4=1 9(c)AFTE	SCHEDULING RESULT (03) (04) (-) (-)	=	i19 i29 i30	PHW=1 001 002 003 004 FIG.	INTRA-HW POINTER Pi1=4 Pi2=1 *Pi3=3 Pi4=4 9(d)AFTE	SCHEDULING RESULT (03) (04) (02) (-) R STEP3	•

INTRA-HW POINTER **SCHEDULING SCHEDULING** INTRA-HW PHW=1 *PHW=2 **RESULT** POINTER RESULT (o3) Pi1=4 (o3)oila °01 i19 **°**01 Pi1=4 i2۹ (o4) ۰i2q 2ەم Pi2=1 ٥<u>0</u>2 Pi 2=2 (o4) i3º (o2) Pi3=3 (o2) **~**03 Pi3=3 i3o ₽03 i40 Pi4=4 (-) Pi4=4 (-) **604** i40 604 FIG. 9(e)AFTER STEP4 FIG. 9(f) AFTER STEP5



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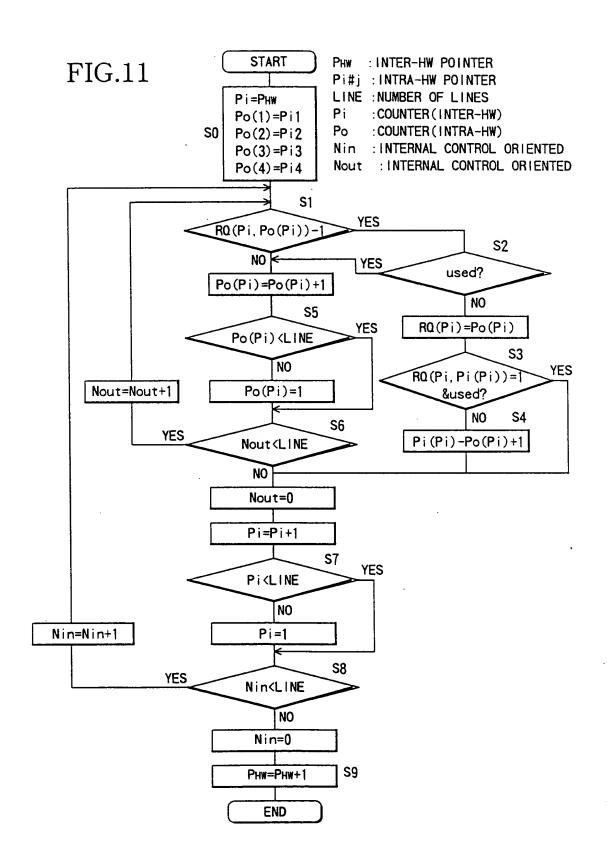
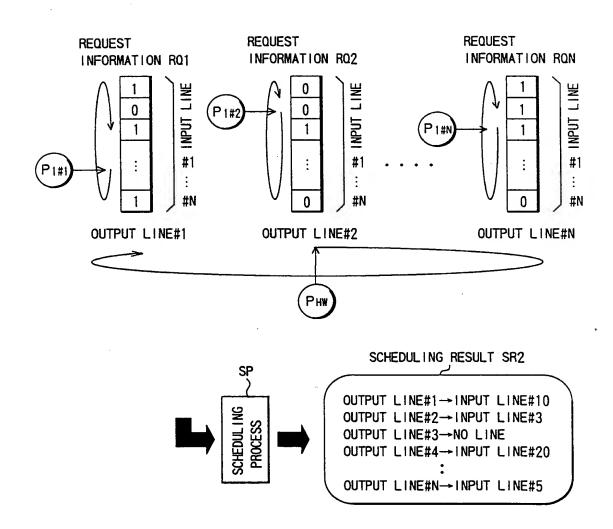


FIG.12



	PHW=1 INTRA-I POINTE i1 001 0 Po1=1 i2 002 Po2=2 i3 003 Po3=3 i4 004 Po4=4 FIG. 13(a) INI (STEP0)	R INFORMATION (i2) 2 (i3, i4) 3 (i1, i2, i3, i4) 4 (i2)	i1° °°01 *P°1=3 (i2) i2° °°02° P°2=2 (-)
→	PHW=1 INTRA-POINTE i10 001 Po1=2 i20 002 *Po2=4 i30 003 Po3=2 i40 004 Po4=4 FIG. 13(c)A	R RESULT 3 (i2) 4 (i3) 3 (-) 4 (-)	PHW=1 INTRA-HW SCHEDULING RESULT i10 001 Po1=3 (i2) i20 002 Po2=4 (i3) i30 003 *Po3=3 (i4) i40 0040 Po4=4 (-) FIG. 13(d) AFTER STEP3
>	PHW=1 NTRA- POINTE i1 ° 001 ° Po1= i2 ° 002 Po2= i3 ° 003 Po3= i4 ° 004 Po4=	R RESULT 3 (i2) 4 (i3) 3 (i4)	*PHW=2 INTRA-HW SCHEDULING RESULT i10 001 Po1=3 (i2) i20 0020 Po2=4 (i3) i30 003 Po3=3 (i4) i40 004 Po4=4 (-)

FIG. 13(f)AFTER STEP5

FIG. 13(e) AFTER STEP4

PHW=2 INTRA-HW REQUEST INFORMATION	PHW=2 INTRA-HW SCHEDULING RESULT i1
(STEP0) PHW=2 INTRA-HW SCHEDULING RESULT i1	PHW=2 INTRA-HW SCHEDULING PHW=2 POINTER RESULT i1

SCHEDUL ING

RESULT (-)

(i4)

(i3)

(i2)

INTRA-HW

Po1=3

Po2=1

Po3=4

Po4=3

FIG. 14(f) AFTER STEP5

POINTER

i10

i2q

i30

14d

°01

902

604

SCHEDUL I NG

RESULT

(-)

(i4)

(i3)

(i2)

INTRA-HW

Po1=3

Po2=1

Po3=4

Po4=3

FIG. 14(e)AFTER STEP4

POINTER

i10

i29

i30

i46

001

ە20م

FIG.15

. ...*\

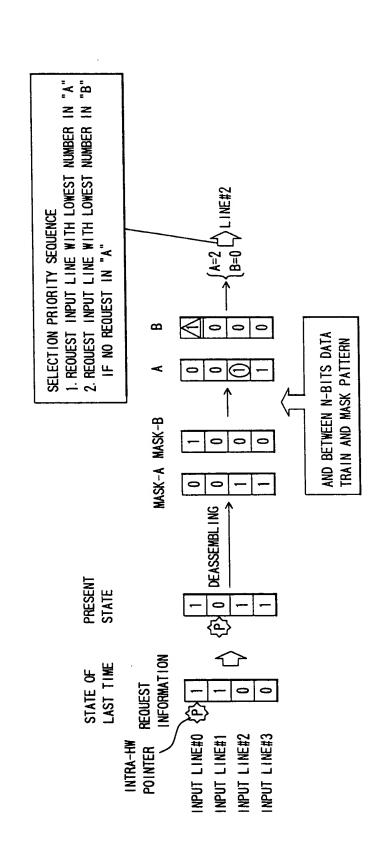


FIG. 16

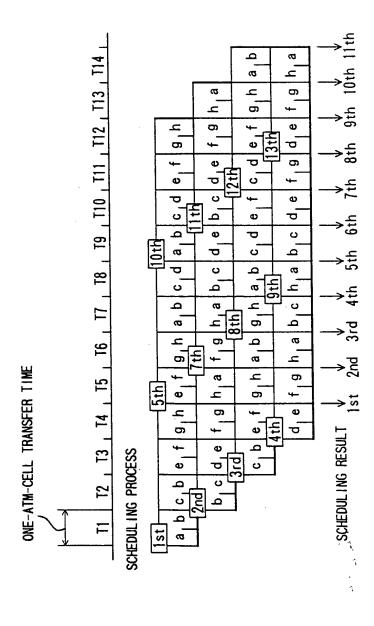
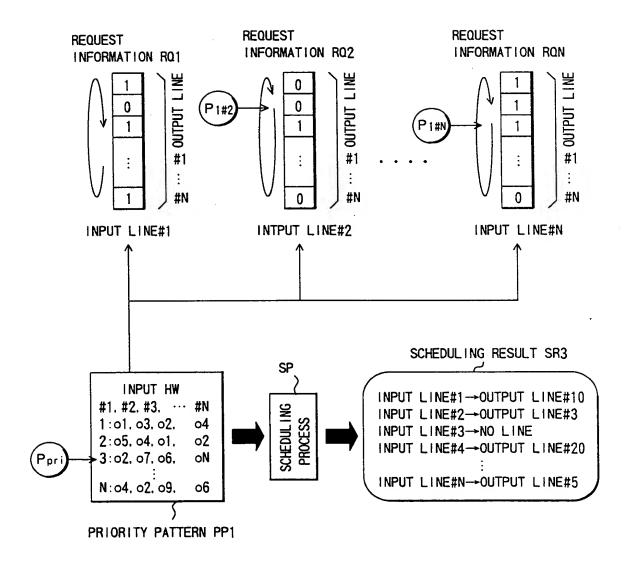


FIG.17



	PRIORTY o Ppri=1 1st 2nd 3rd 4th	REQUEST INFORMATION	PRIORTY SCHEDULING Ppri=1 1st 2nd 3rd 4th RESULT
	i1 o o1 o3 o2 o4 i2 o2 o4 o2 o1 o3 i3 o3 o1 o4 o2 i4 o2 o4 o3 o1	(01, 02)	i1 ° ° ° ° ° ° ° ° ° ° ° ° ° ° ° ° ° ° °
	FIG. 18(a)INITIAL ST (STEPO)	ATE	FIG. 18(b) AFTER STEP1
	PRIORTY Ppri=1 1st 2nd 3rd 4th	SCHEDULING RESULT	PRIORTY SCHEDULING Ppri=1 1st 2nd 3rd 4th RESULT
→	i1	(o3) (-) (o1) (o2)	i1
•	FIG. 18(c)AFTER ST	EP2	FIG. 18(d)AFTER STEP3
	PRIORTY o Ppri=1 1st 2nd 3rd 4th	SCHEDUL I NG RESULT	PRIORTY SCHEDULING *Ppri=1 1st 2nd 3rd 4th RESULT
→	i1	(o3) (-) (o1) (o2)	i1
	FIG. 18(e)AFTER ST	EP4	FIG. 18(f)AFTER STEP5

	PRIORTY Ppri=21st 2nd 3rd 4th	REQUEST INFORMATION	PRIORTY SCHEDULING Ppri=21st 2nd 3rd 4th RESULT			
	i2 02 04 02 01 03	(o3) (o1, o2) (o2, o4) (o3)	i10			
	FIG. 19(a)INITIAL ST (STEPO)	TATE	FIG. 19(b) AFTER STEP1			
	PRIORTY Ppri=21st 2nd 3rd 4th	SCHEDUL ING RESULT	PRIORTY SCHEDULING Ppri=2 1st 2nd 3rd 4th RESULT			
→		(o3) (o2) (o4) (-)	i1			
	FIG. 19(c)AFTER ST	EP2	FIG. 19(d)AFTER STEP3 .			
	PRIORTY Ppri=2 1st 2nd 3rd 4th	SCHEDUL I NG RESULT	PRIORTY SCHEDULING *Ppri=3 1st 2nd 3rd 4th RESULT			
>	i1 ° ° ° ° ° ° ° ° ° ° ° ° ° ° ° ° ° ° °	(o3) (o2) (o4) (-)	i1			
	FIG. 19(e)AFTER ST	TEP4	FIG. 19(f)AFTER STEP5			

Ppri : PRIORITY POINTER

Pno : COUNTER (PRIORITY PATTERN No.)

FIG.20 LINE : NUMBER OF LINES

PT :PRIORITY PATTERN VALUE

i :INTERNAL CONTROL ORIENTED

Nno :INTERNAL CONTROL ORIENTED

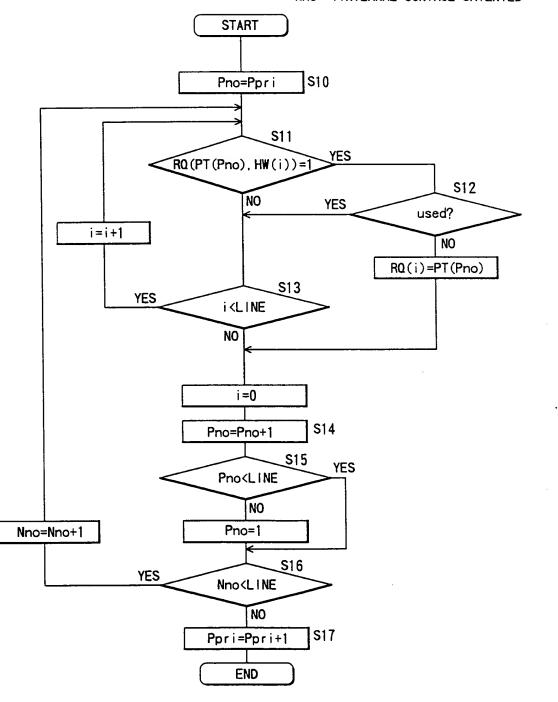
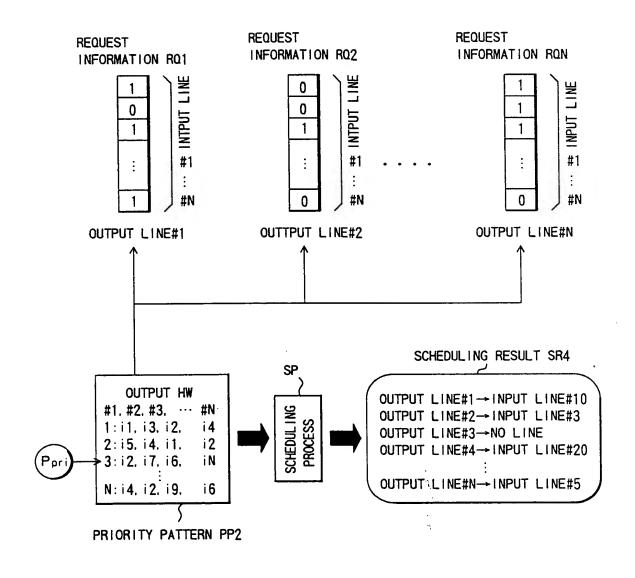


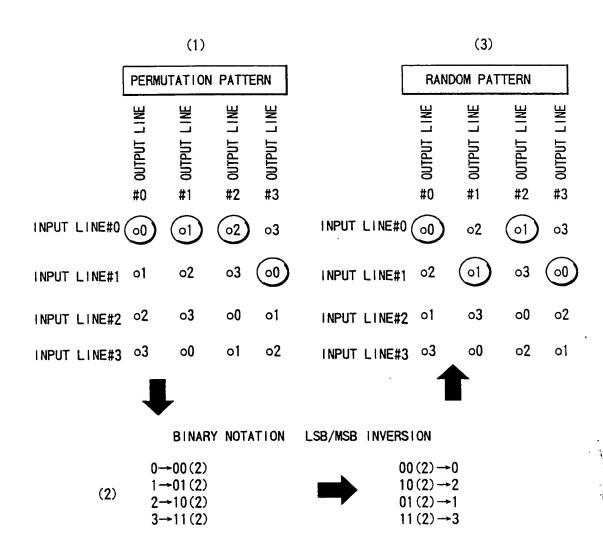
FIG.21



	PRIORTY	REQUEST	PRIORTY SCHEDULING	i
	Ppri=1 1st 2nd 3rd 4th	INFORMATION	Ppri=1 1st 2nd 3rd 4th RESULT	
	i1 a oo1 i1 i3 i2 i4	(i2) (i2, i3, i4),	i1	
	i2 02 i4 i2 i1 i3 i3 03 i3 o1 i4 i2	(i2, i4)	i3° /°03 i3 i1 i4 i2 (-)	
	i4 04 i2 i4 i3 i1	(i3)	i40 oo4 i2 i4 i3 i1 (-)	
	FIG. 22(a)INITIAL ST (STEPO)	`ATE	FIG. 22(b) AFTER STEP1	
	PRIORTY		PRIORTY SCHEDULING	ì
	Ppri=1 1st 2nd 3rd 4th	SCHEDULING RESULT	Ppri=1 1st 2nd 3rd 4th RESULT	•
	i19 po1 *i1 i3 i2 i4	(i3)	i19 po1 i1 i3 i2 i4 (i3)	
	i2° × °°° 14 i2 i1 i3	(i4)	120 002 14 12 11 13 (14)	
7	i30 003 *i3 i1 i4 i2 i40 004 i2 i4 i3 i1	(i1) 7	i30 003 i3 i1 i4 i2 (i1) 7 i40 004 i2 i4 i3 i1 (-)	
	140 004 12 14 13 11	()		
	FIG. 22(c)AFTER S	TEP3	FIG. 22(d)AFTER STEP4	
	PRIORTY	COUEDUIL INC	PRIORTY SCHEDULING	3
	Ppri=1 1st 2nd 3rd 4th	SCHEDULING RESULT	*Ppri=1 1st 2nd 3rd 4th RESULT	
	i19 001 i1 i3 i2 i4	(i3)	i19 001 i1 i3 i2 i4 (i3)	
_	i2° × 02 i4 i2 i1 i3	(i4)	i2° × 02 i4 i2 i1 i3 (i4)	
-	i30 003 i3 i1 i4 i2	(i1) –	i30 oo3 i3 i1 i4 i2 (i1)	
	i4d ∘o4 i2 i4 i3 i1	(-)	i4d oo4 i2 i4 i3 i1 (-)	
	FIG. 22(e)AFTER S	TEP4	FIG. 22(f) AFTER STEP5	

	PRIORTY Ppri=21st 2° nd 3° rd 4° th	REQUEST INFORMATION	PRIORTY SCHEDULING Ppri=21st 2nd 3rd 4th RESULT		
	i2 02 i4 i2 i1 i3 i3 03 i3 o1 i4 i2 i4 04 i2 i4 i3 i1 FIG. 23(a) INITIAL ST	(i3)	i1		
	(STEP0) PRIORTY Ppri=21st 2nd 3rd 4th	SCHEDUL I NG RESULT	PRIORTY SCHEDULING Ppri=2 1st 2nd 3rd 4th RESULT		
→		(-) (i2) (i1) (i3)	i1 o oo1 i1 i3 i2 i4 (-) i2 o oo2 i4 i2 i1 i3 (i2) i3 o oo3 i3 i1 i4 i2 (i1) i4 o oo4 i2 i4 i3 i1 (i3)		
	FIG. 23(c)AFTER ST	EP3	FIG. 23(d) AFTER STEP4		
	PRIORTY Ppri=2.1st 2nd 3rd 4th	SCHEDUL I NG RESULT	PRIORTY SCHEDULING **Ppri=31st 2nd 3rd 4th RESULT		
→	il o ool il i3 i2 i4 i2 o oo2 i4 i2 il i3 i3 o oo3 i3 il i4 i2 i4 o oo4 i2 i4 i3 il FIG. 23(e) AFTER ST	(-) (i2) (i1) (i3)	ile ool il i3 i2 i4 (-) i2o oo2 i4 i2 il i3 (i2) i3o oo3 i3 il i4 i2 (il) i4o oo4 i2 i4 i3 il (i3) FIG 23(f) AFTER STEP5		
	rio. 20(e) arien Si	FIG. 23(f)AFTER STEP5			

FIG.24



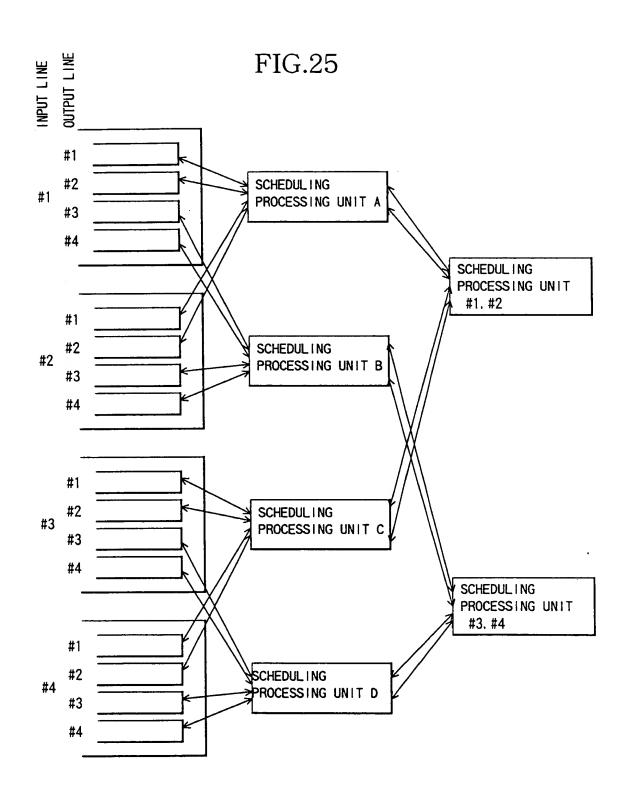


FIG.26 (a)

TENTATIVE CANDIDATE SELECTION IN SCHEDULING PROCESSING UNIT A

	PRIORTY				PRIORTY	
		SCHEDULING	•			SCHEDUL ING
	1st 2nd	RESULT			1st 2nd	RESULT
i1⊶—•o1	o1 o2	(01)	_	i1∘ ->∘ o1	o1 o2	(01)
i202	o 2 o1	(o2)		i2 ∘> ∘2	o2 o1	(o2)

TENTATIVE CANDIDATE SELECTION IN SCHEDULING PROCESSING UNIT B

		PRIORTY	CCUEDUI II				PRIORTY	COUEDUILLING
		1st 2nd	SCHEDUL I NO RESULT	NO			SCHEDUL I NG RESULT	
i1•	 ∘o3	o3 o4	(o3)	_	i1⊶	→ 03	o3 o4	(03)
i2°	oo4	o4 o3	(-)		i2°	904	o4 o3	(-)

TENTATIVE CANDIDATE SELECTION IN SCHEDULING PROCESSING UNIT C

		PRIORTY	001150111111	o			PRIORTY	
		1st 2nd	SCHEDUL I I RESULT	NG	ı		1st 2nd	SCHEDULING RESULT
i3°	° 01	01 02	(-)	_	i3°	° 01	o1 o2	(-)
i40	°02	02 01	(-)	-	i40	° 02	o2 o1	(-)

TENTATIVE CANDIDATE SELECTION IN SCHEDULING PROCESSING UNIT D

	PRIORTY					PRIORTY	
	$1st \frac{0}{2}nd$	SCHEDUL ING RESULT				1st 2nd	SCHEDUL ING RESULT
i3⊶_∞o3	03 04	(o3)	_	i3⊶	-> ∘o3	03 04	(03)
i40 004	o4 o3	(o3)	7	i4°	°04	o4 o3	(-)

FIG.26 (b)

PRIORTY	SCHEDUL ING	PRIORTY	SCHEDULING
1st 2nd 3rd 4th		1st 2nd 3rd 4th	RESULT
i1 ~ 01 o1 o3 o2 o4	(o1, o3)	i1∘>∘o1 o3 o4 o1 o2	(o1)
i2° \ 02 02 01 04 03	(02)	i2°→∞02 o4 o3 o2 o1	
i3 03 04 01 02	(o3)	i3 0→∞ 03 o1 o2 o3 o4	(o3)
i4° °04 04 03 02 01		i4° °04 02 01 04 03	

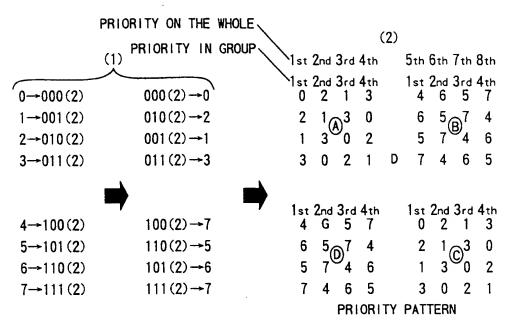
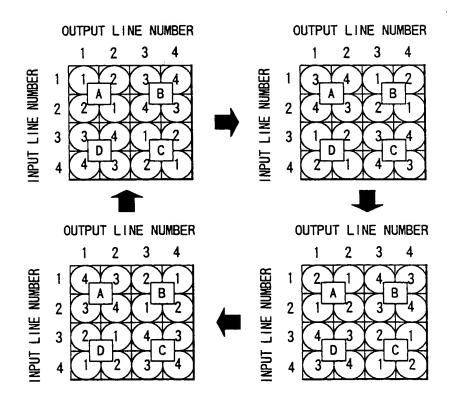
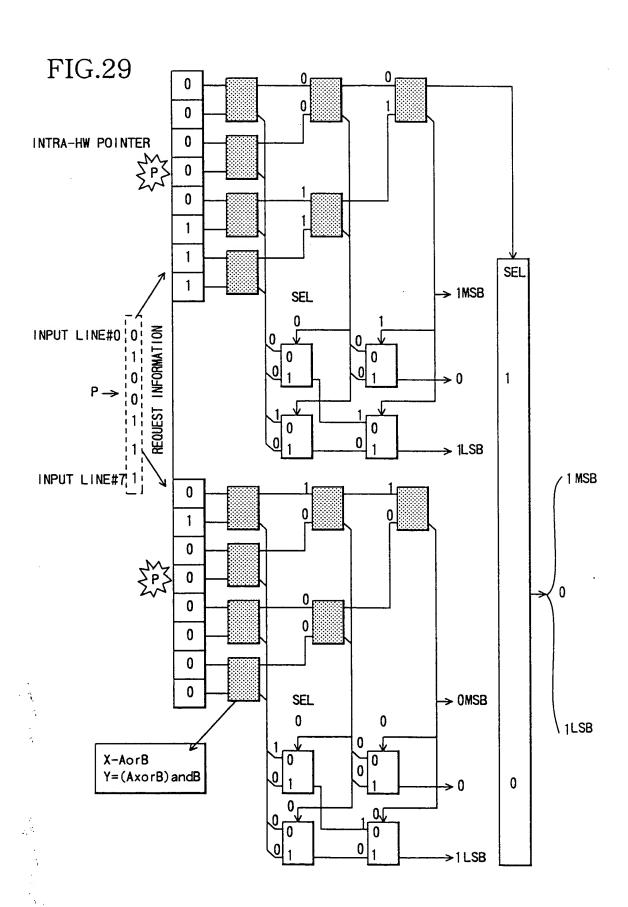
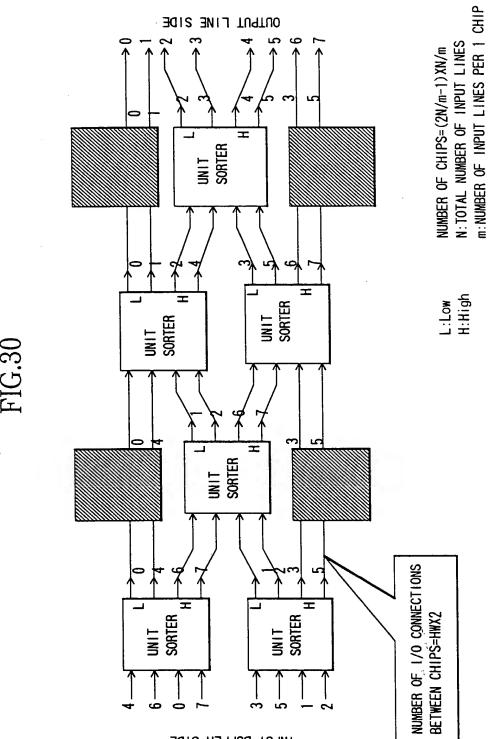


FIG.28

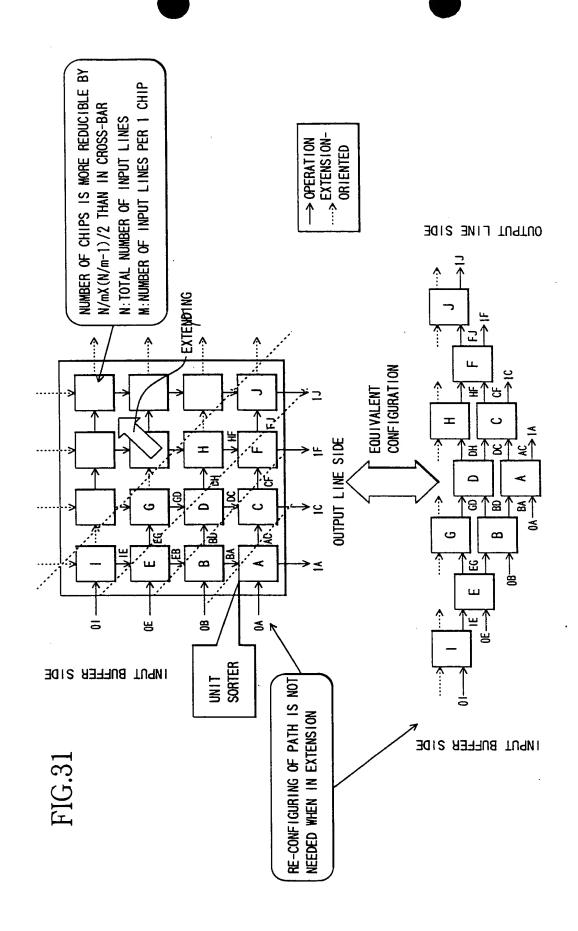


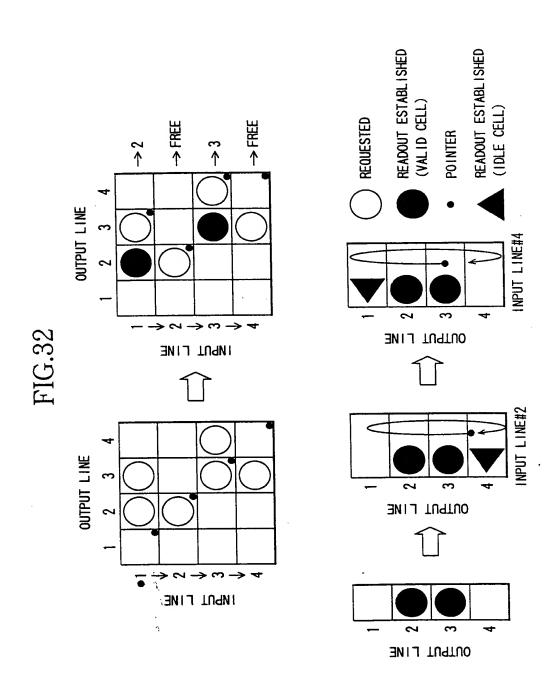


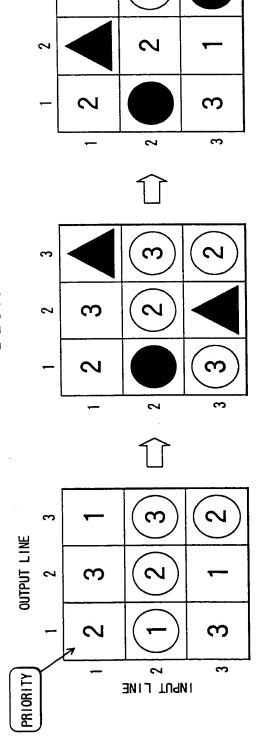


INPUT BUFFER SIDE

OUTPUT LINE SIDE







3

SAME PROCESSES ARE REPEATED ITH AS FOR PRIORITY 3

O:DATA EXISTING

:READOUT ESTABLISHED

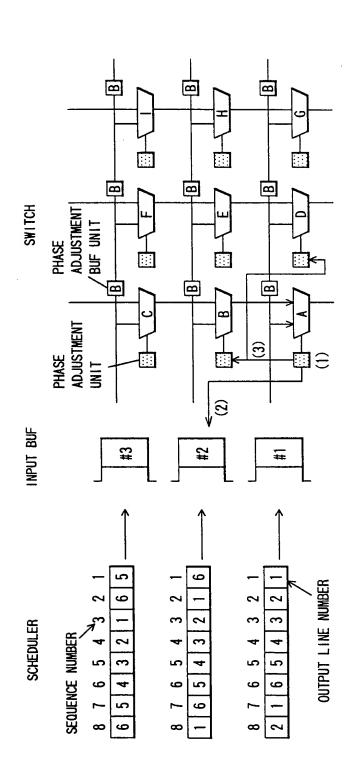
(VALID CELL)

★:READOUT TENTATIVELY
ESTABLISHED (IDLE CELL)

CONCERNING PRIORITY 1:VALID
CELL ESTABLISHMENT IS MADE WHEN
DATA EXISTS, IDLE CELL TENTATIVE
ESTABLISHMENT IS MADE WHEN NO
DATA EXISTS

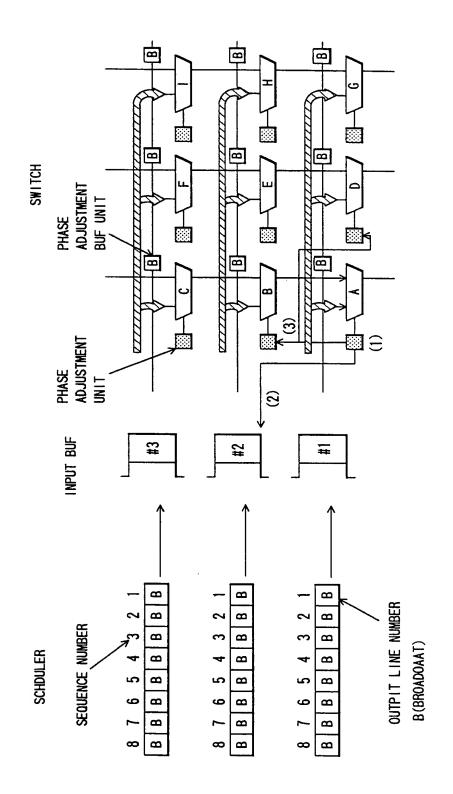
CONCERNING PRIORITY 2:ESTABLISHMENT IS
MADE WHEN DATA EXIST AND VALID CELL WITH
PRIORITY 1 OF SAME 1/0 LINE IS NOT YET
ESTABLISHED TENTATIVE ESTABLISHMENT IS
RULED OUT WHEN DATA EXISTS AND IDLE CELL
WITH PRIORITY 1 OF SAME 1/0 LINE IS
ESTABLISHMENT FOR IDLE CELL IS MADE WHEN
NO DATA EXISTS, AND WHEN NEITHER
ESTABLISHMENT NOR TENTATIVE
ESTABLISHMENT IS MADE IN SAME 1/0 LINE

FIG.34



	SCHEDULER UNIT	INPUT LINE NUMBER	DELAY COMPONENT (INPUT BUFFER)	INPUT TO SW
T=0	8 7 6 5 4 3 2 1 3 2 1 3 2 1 3 2 8 7 6 5 4 3 2 1 1 3 2 1 3 2 1 3 8 7 6 5 4 3 2 1	#3 #2	3 2	
	2 1 3 2 1 3 2 1	#1	1	
	9 8 7 6 5 4 3 2 1 3 2 1 3 2 1 3 9 8 7 6 5 4 3 2	#3	3	
T=1	9 8 7 6 5 4 3 2	#2	2	1 START OF PHASE
	3 2 1 3 2 1 3 2	#1	1 .	ADJUSTMENT △T=0, SW=1
	10 9 8 7 6 5 4 3 2 1 3 2 1	#3	3	
T=2	10 9 8 7 6 5 4 3 3 2 1 3 2 1 3 2	#2	2	3
	10 9 8 7 6 5 4 3	#1	1	$\frac{2}{2}$ $\triangle T=1$, SW=1
	11 10 9 8 7 6 5 4	#3	3	$\frac{1}{2}$
T=3	11 10 9 8 7 6 5 4 1 3 2 1 3 2 1 3 11 10 0 8 7 6 5 4	#2	2	PHASE ADJUSTMENT
	11 10 9 8 7 6 5 4	#1	1	$\frac{3}{3} = \triangle SW - \triangle T = -1$ $\frac{3}{3} \triangle T = 2, SW = 1, \triangle SW = 2 - 1 = 1$
	12 11 10 9 8 7 6 5	#3	3	2 3 DISCARD CELL WHEN
T=4	12 11 10 9 8 7 6 5 2 1 3 2 1 3 2 1 12 11 10 9 8 7 6 5	#2	1=2-1	REDUCING PHASE DIFFERENCE
	3 2 1 3 2 1 3 2	#1	1	1 DITT ENENCE
	13 12 11 10 9 8 7 6	#3	3	3
T=5	13 12 11 10 9 8 7 6 3 2 1 3 2 1 3 2	#2	2	6 START OF PHASE
	13 12 11 10 9 8 7 6 1 3 2 1 3 2 1 3	#1	1	5 DIFFERENCE
	14 13 12 11 10 9 8 7	#3	1=3-2	6 DISCARD CELL WHEN
T=6	14 13 12 11 10 9 8 7	#2	2	REDUCING PHASE DIFFERENCE
	14 13 12 11 10 9 8 7 2 1 3 2 1 3 2 1	#1	1	6 COMPLETION OF PHASE ADJUSTMENT





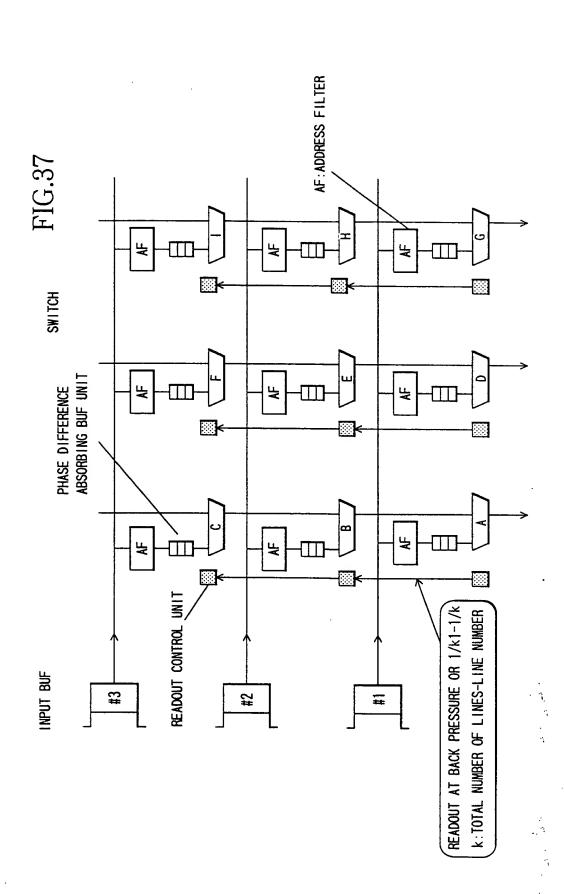


FIG.38

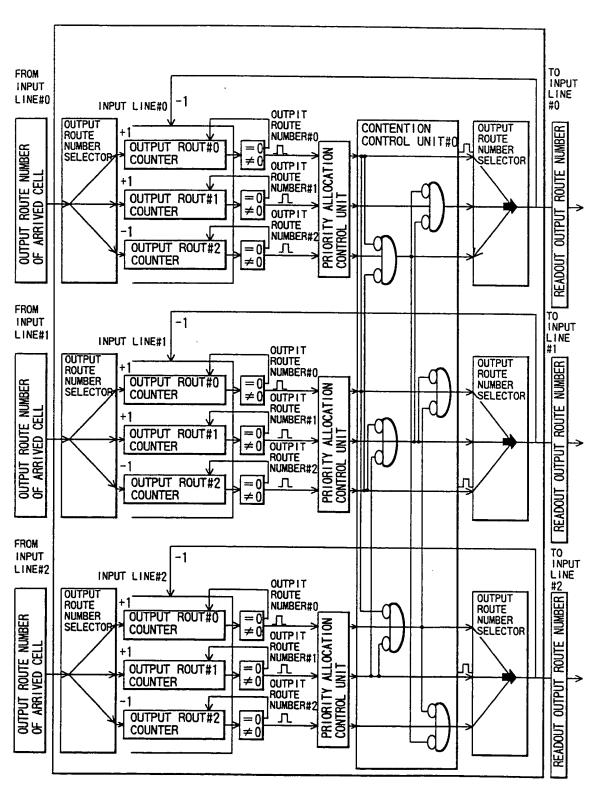


FIG.39

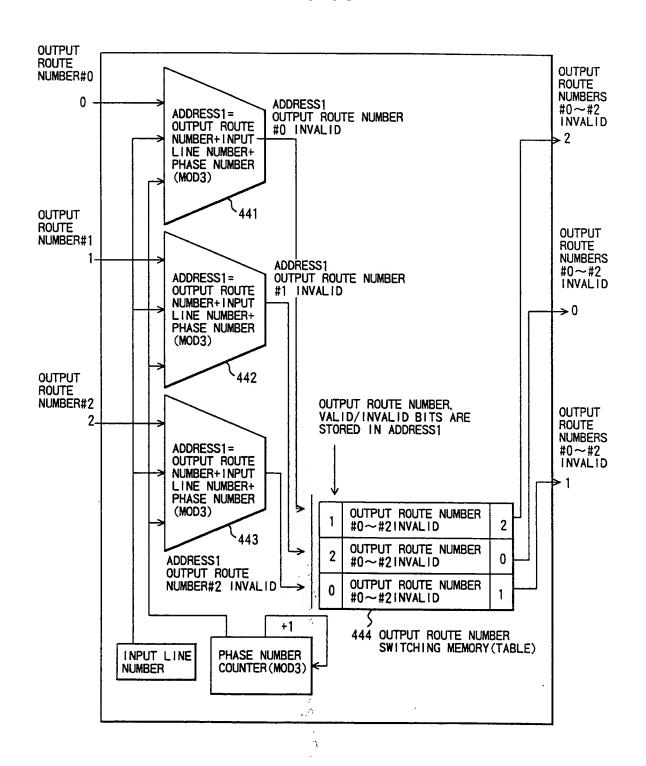


FIG.40

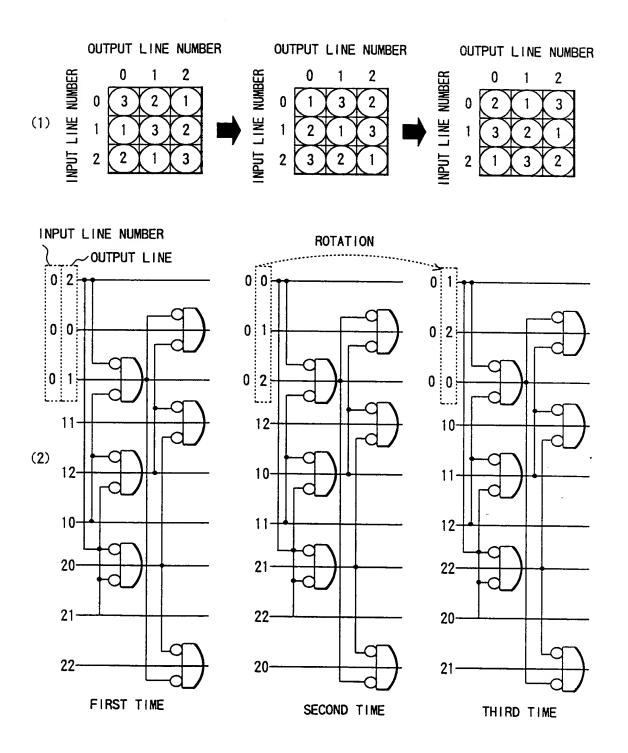


FIG.41

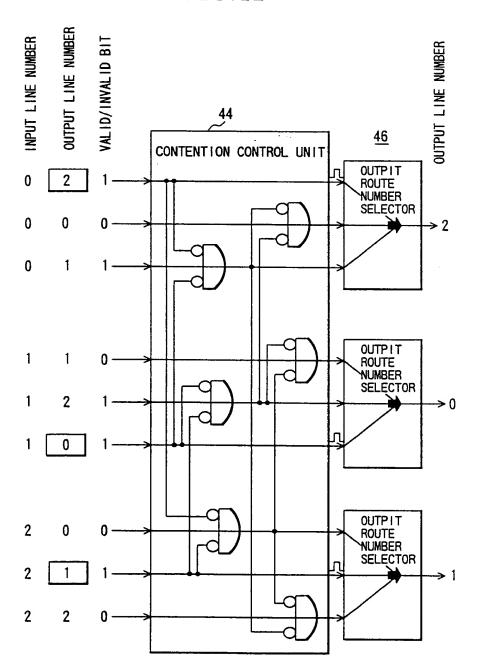
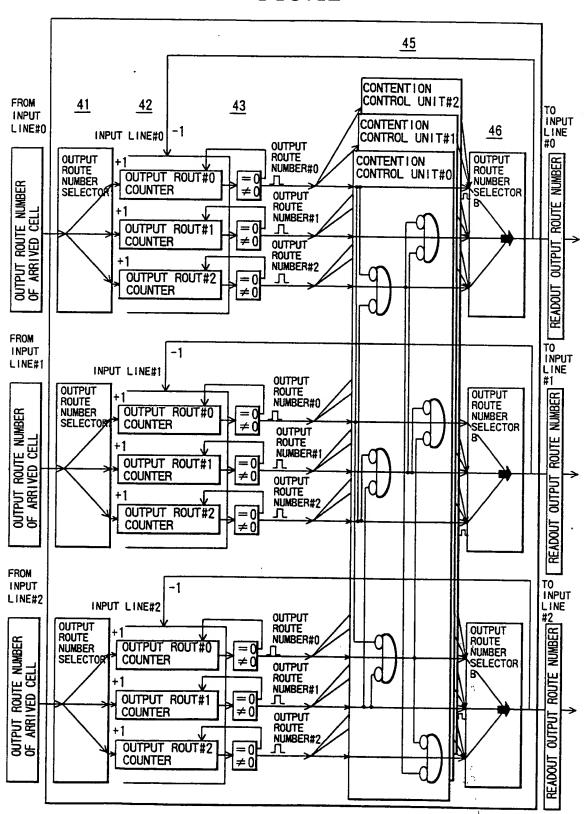


FIG.42



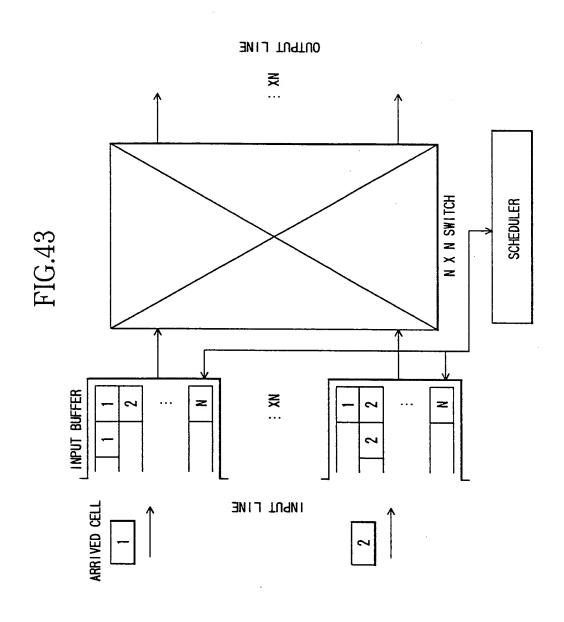
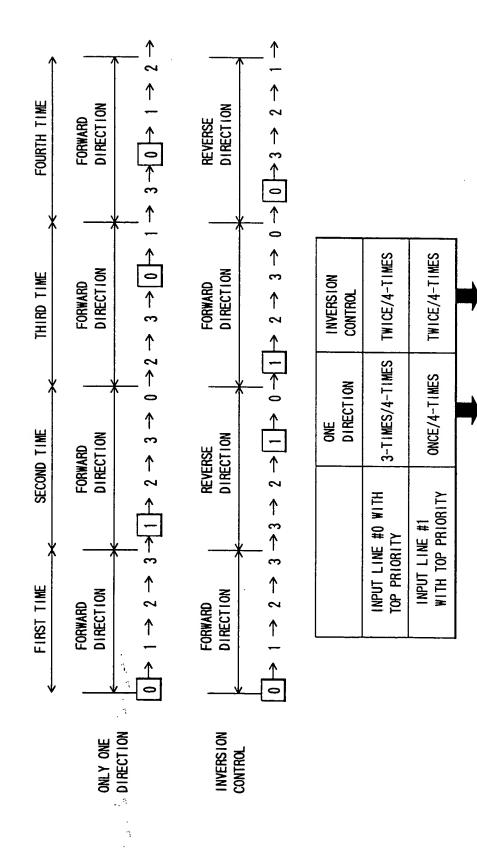


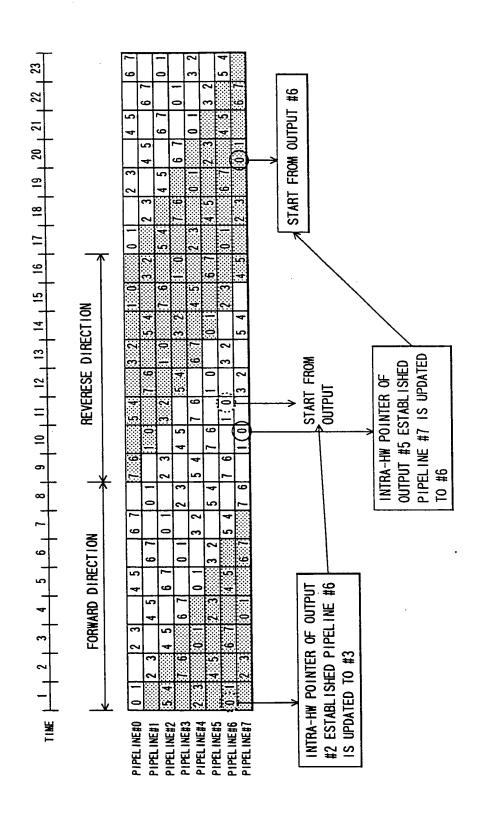
FIG.44



EOUAL

UNEOUAL

FIG.45



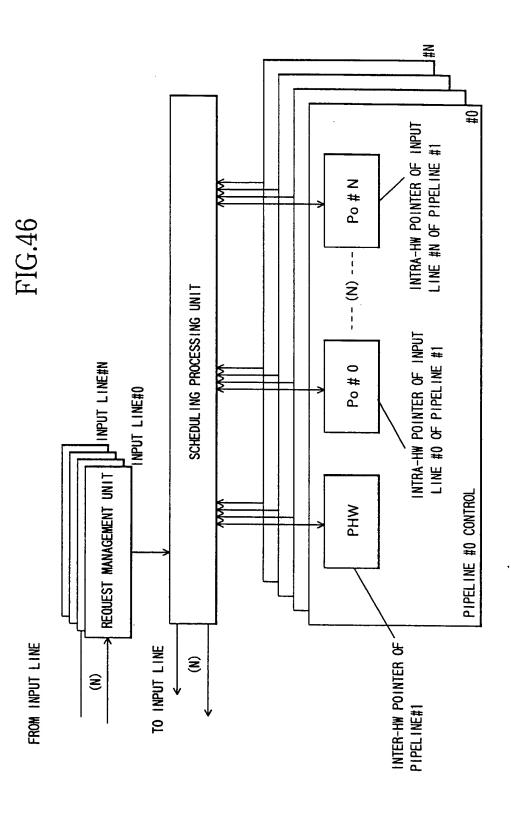
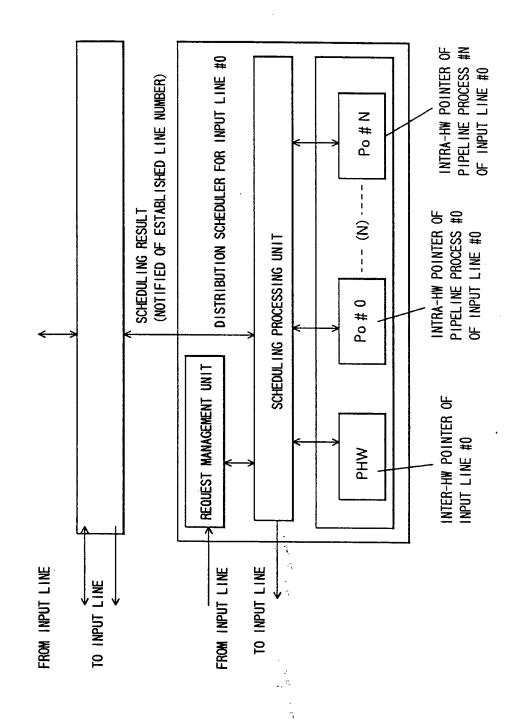
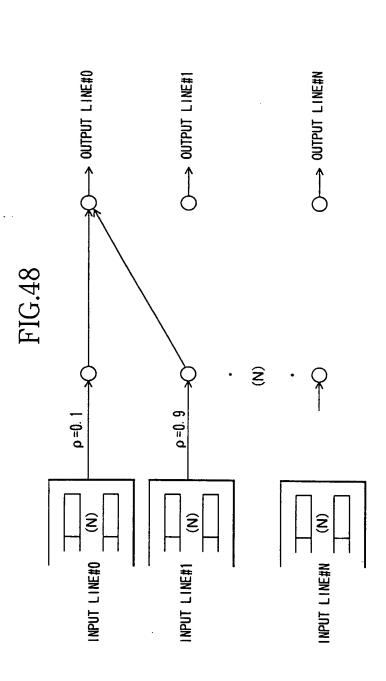


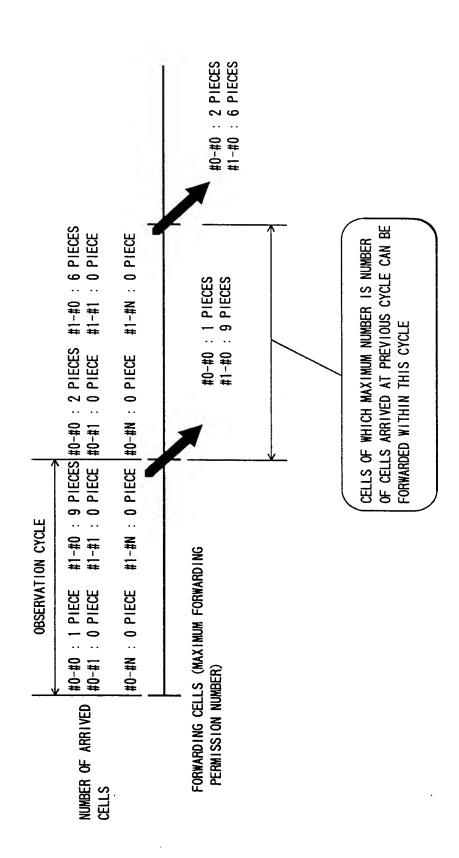
FIG.47

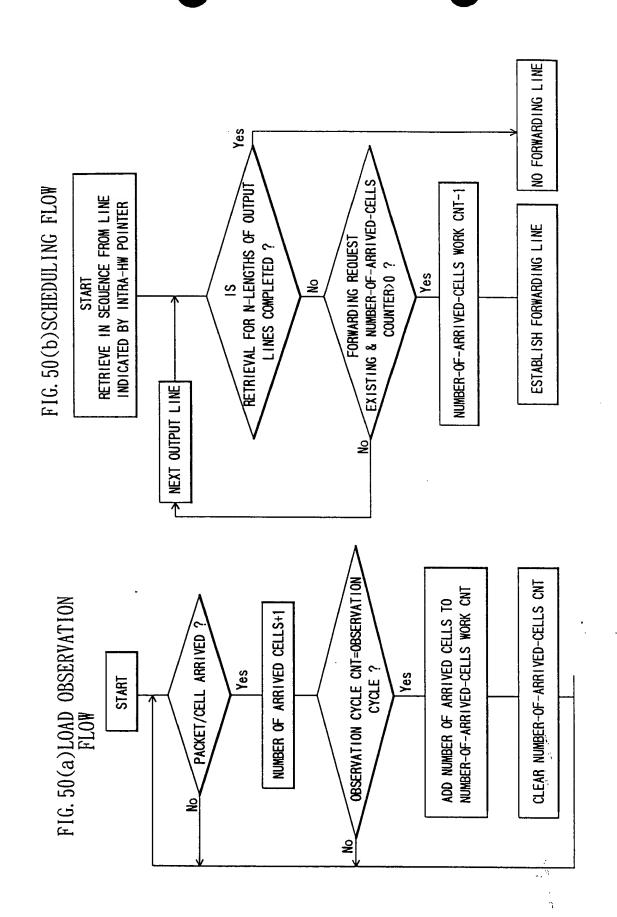


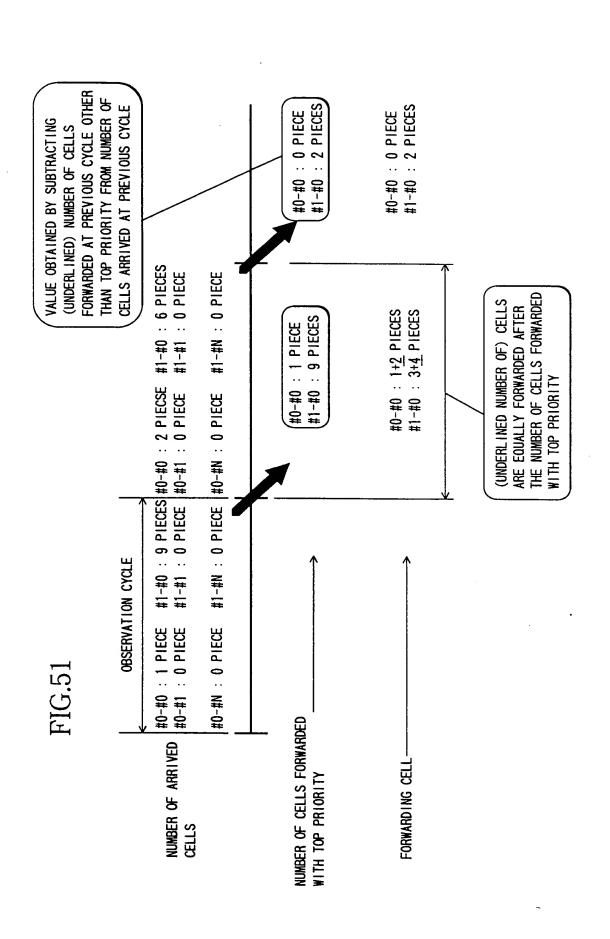


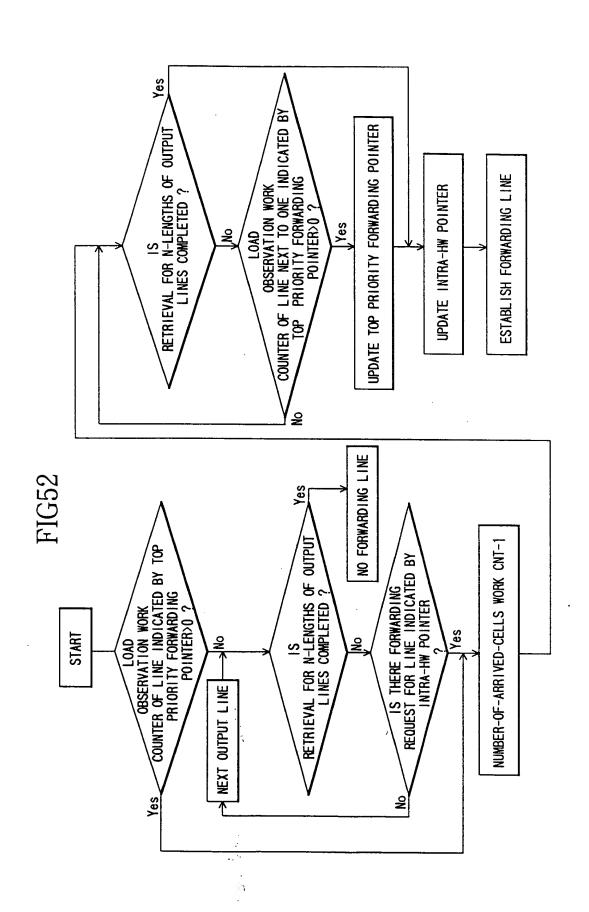
PATH:#1-#0 SELECTION PROBABILITY:0.5→INPUT LOAD 0.9→INCREASED QUEUE LENGTH PATH:#0-#0 SELECTION PROBABILITY:0.5→INPUT LOAD 0.1→NO PROBLEM

FIG.48









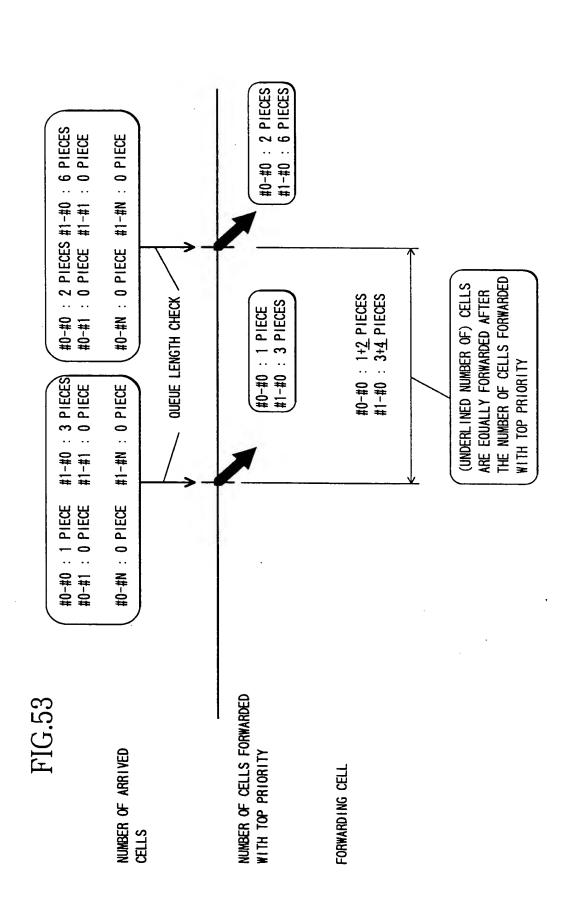
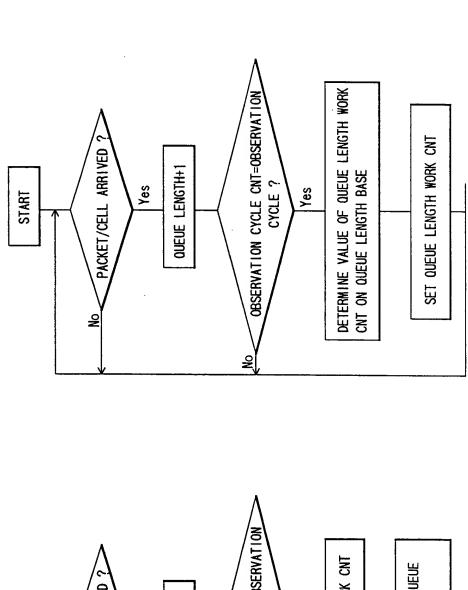
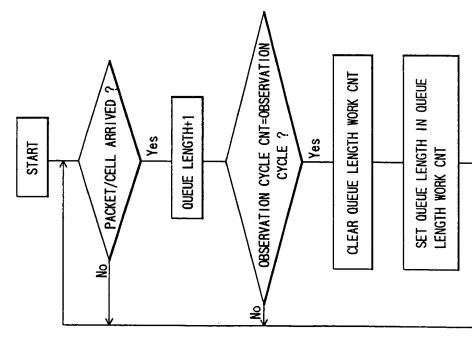


FIG. 54(a)LOAD OBSERVATION FLOW ON

BASED ON QUEUE LENGTH BASE (PART 2) FIG. 54(b)(c)LOAD OBSERVATION FLOW QUEUE LENGTH BASE (PART 1)





a) MEASURED RESULTS ARE SET INTACT

PATH#0-PATH#0 QUEUE LENGTH: 10P1ECES→10 PATH#1-PATH#0 QUEUE LENGTH: 2P1ECES→1 PATH#2-PATH#0 QUEUE LENGTH: 5P1ECES→3

PATH#3-PATH#0 QUEUE LENGTH: 10PIECES→10

b) FORWARDING RATE AT NEXT CYCLE IS DETERMINED AT RATE OF QUEUE LENGTH(EXAMPLE:FIXED CYCLE=20-PACKET TIME

PATH#0-PATH#0 QUEUE LENGTH:10P1ECES→10/(10+2+5+10)*20=7.4=7
PATH#1-PATH#0 QUEUE LENGTH:2P1ECES→2/(10+2+5+10)*20=1.4=1
PATH#2-PATH#0 QUEUE LENGTH:5P1ECES→5/(10+2+5+10)*20=3.7=3

PATH#3-PATH#0 QUEUE LENGTH: 10P1ECES→10/(10+2+5+10)*20=7. 4=7

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FORWARDING RATE AT NEXT CYCLE IS DETERMINED CORRESPONDING TO QUEUE LENGTH(EXAMPLE:FIXED CYCLE=20-PACKET TIME — RANGE AND RATE MAY BE ARBITRARILY SET

OUEUE LENGTH: $1 \sim 3 \rightarrow 0$. $05 * 20 \rightarrow 1$ OUEUE LENGTH: $3 \sim 10 \rightarrow 0$. $1 * 20 \rightarrow 2$ OUEUE LENGTH: $10 \sim 20 \rightarrow 0$. $2 * 20 \rightarrow 4$ OUEUE LENGTH: $20 \sim 30 \rightarrow 0$. $3 * 20 \rightarrow 6$

QUEUE LENGTH:90~100→1.0*20→20

PATH#0-PATH#0 QUEUE LENGTH:10PIECES→2 PATH#1-PATH#0 QUEUE LENGTH:2PIECES→1

PATH#3-PATH#0 QUEUE LENGTH:10P1ECES→2 PATH#2-PATH#0 QUEUE LENGTH: 5PIECES→2

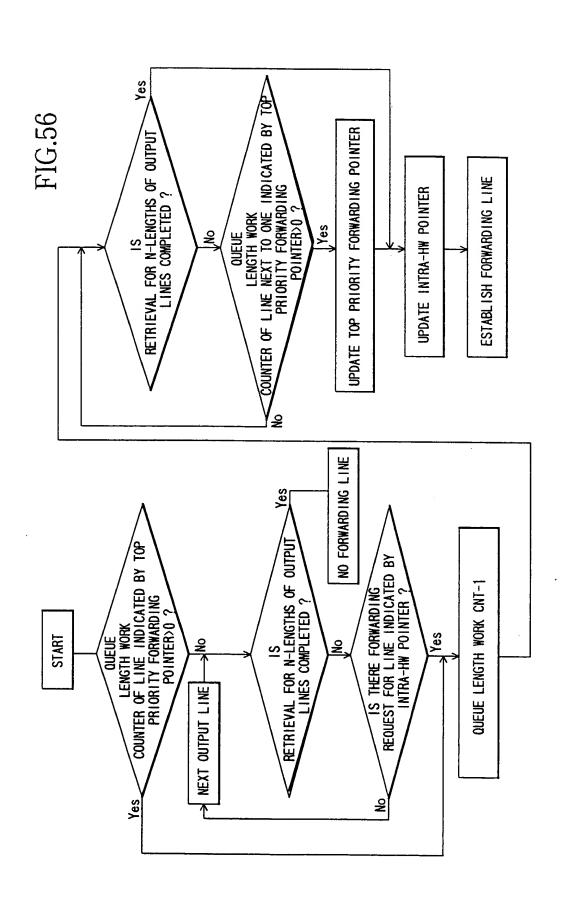
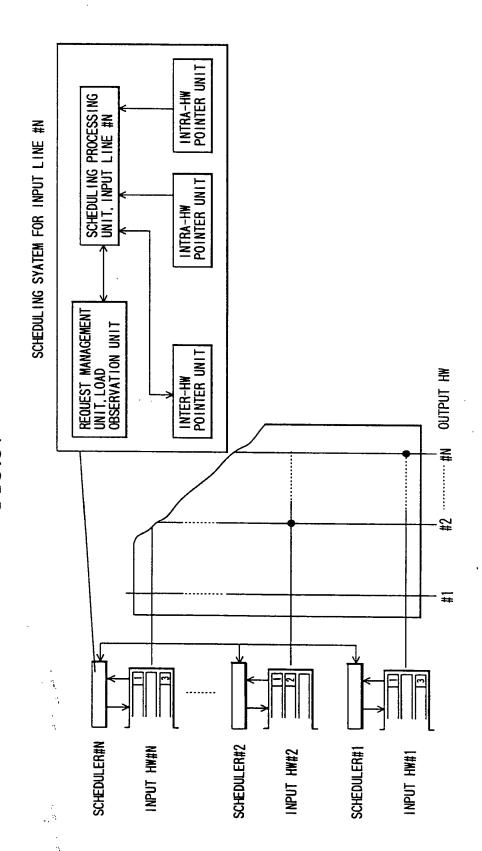
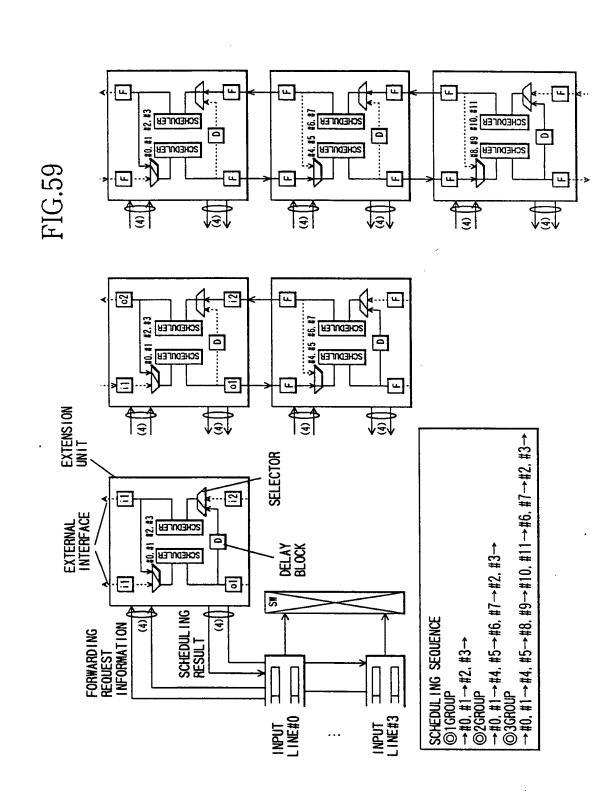
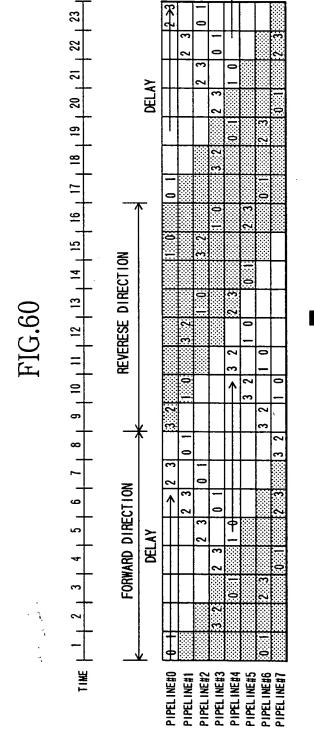


FIG.57



AFTER EXTENSION FIG. 58(b) TANDEM CONNECTION (4) | INPUT LINE#3 ---> INPUT LINE#0 ---INPUT LINE#8 — INPUT LINE#7 -INPUT LINE#4 -INPUT LINE#11-BEFORE Extension (4) INPUT LINE#3 —> (4) | INPUT LINE#7 ──> INPUT LINE#0 ---INPUT LINE#4 ---AFTER Extension (4) | INPUT LINE#4 —>
(4) FIG. 58(a)RING CONNECTION (4) |NPUT LINE#11---> INPUT LINE#8 ---> INPUT LINE#0 ---BEFORE Extension SCHEDULER (INPUT ROUTE#7) (4) INPUT LINE#3 —> (4) INPUT LINE#7 —> INPUT LINE#4 ---> INPUT LINE#0 ----





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FIG.61

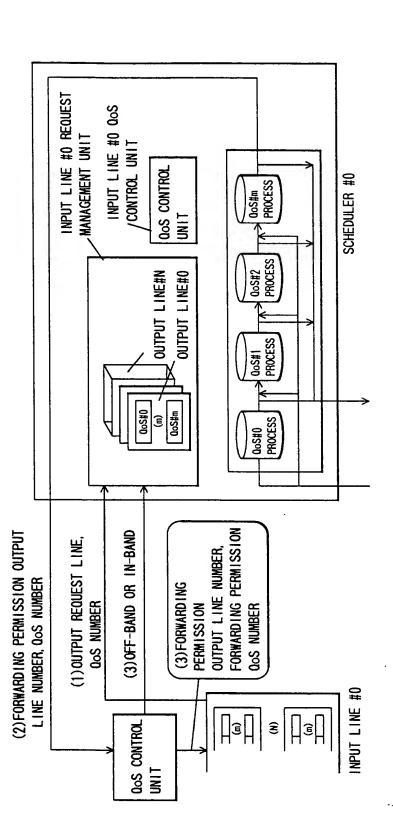
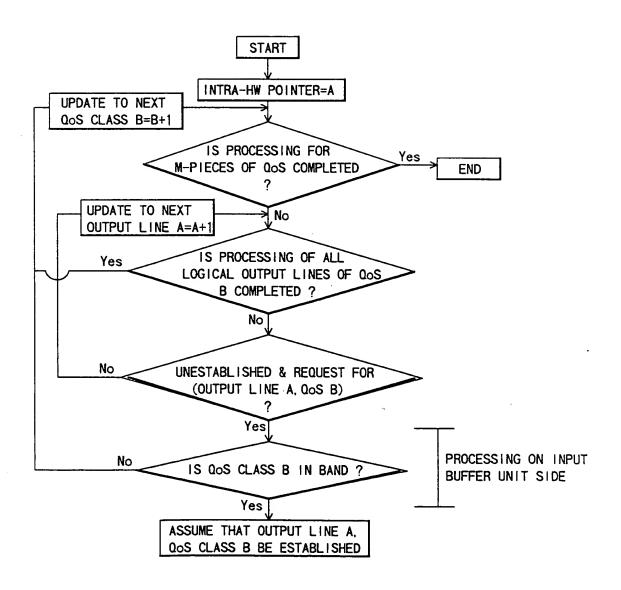


FIG.62



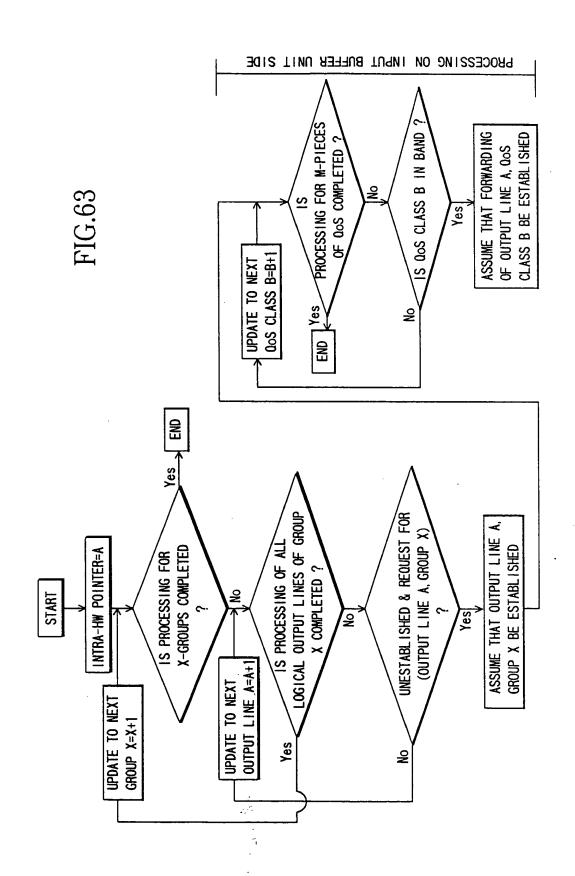
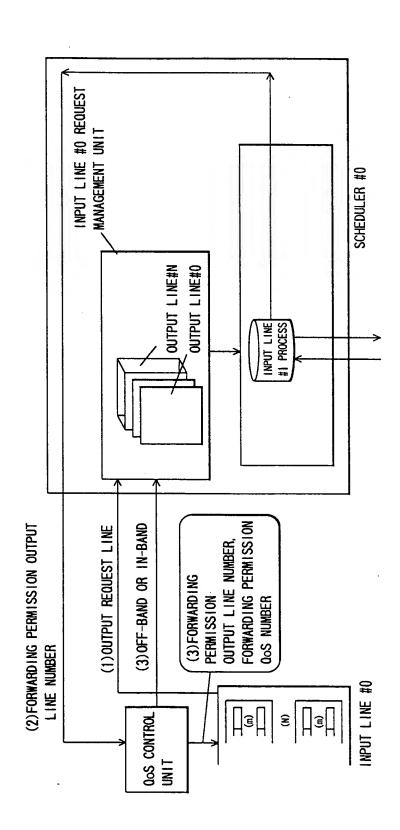


FIG.64



PROCESSING ON INPUT BUFFER UNIT SIDE PROCESSING FOR M-PIECES IS GOS CLASS B IN BAND ASSUME THAT FORWARDING CLASS B BE ESTABLISHED OF Dos COMPLETED 2 OF OUTPUT LINE A, GoS 2 Kes 0oS CLASS B=B+1 UPDATE TO NEXT END LYes 운 읆 Yes UNESTABLISHED & REQUEST FOR ALL LOGICAL OUTPUT LINES LINE A, BE ESTABLISHED INTRA-HW POINTER=A OUTPUT LINE A ? IS PROCESSING OF ASSUME THAT OUTPUT COMPLETED ? ટ START Yes OUTPUT LINE A=A+1 UPDATE TO NEXT ₽

FIG.65

FIG.66

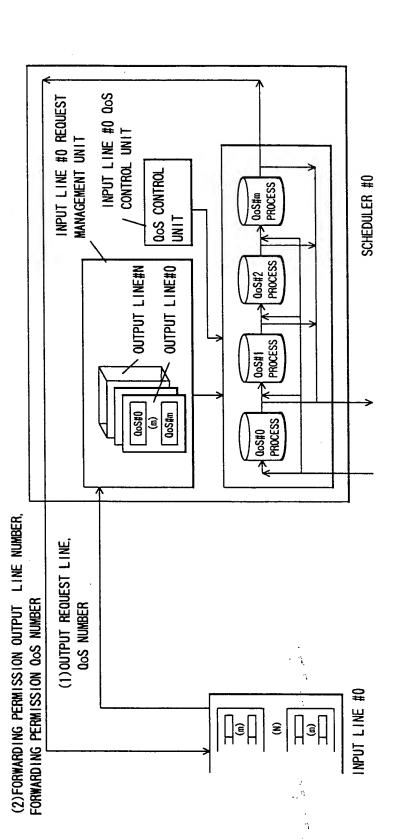


FIG.67

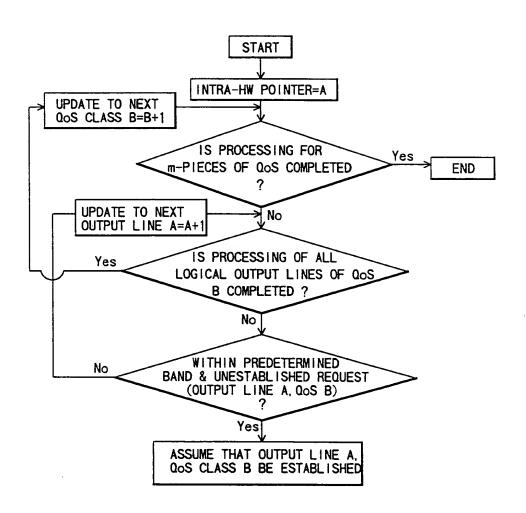


FIG.68

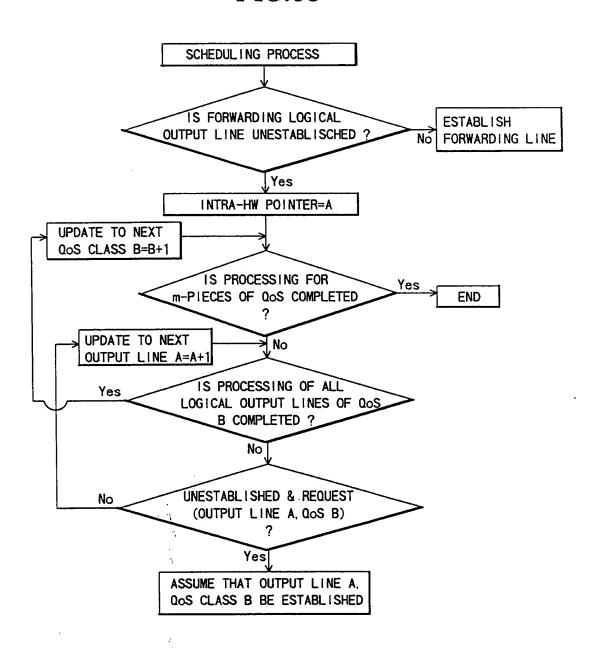
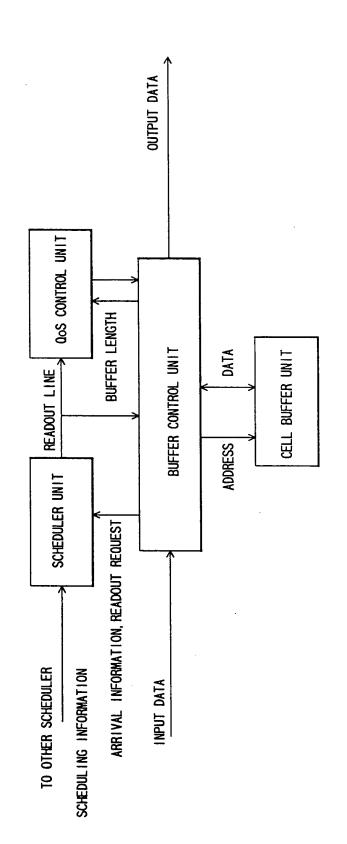
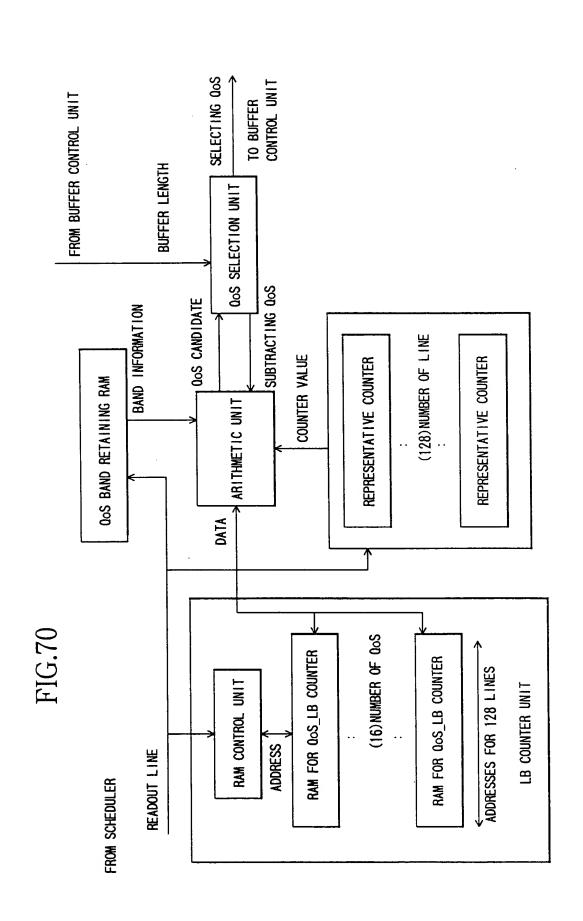
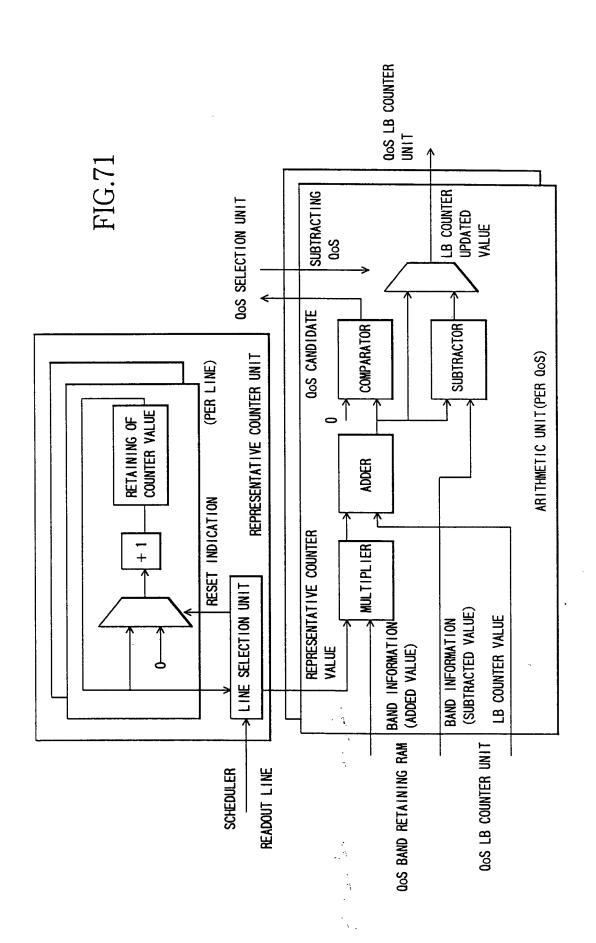


FIG.69







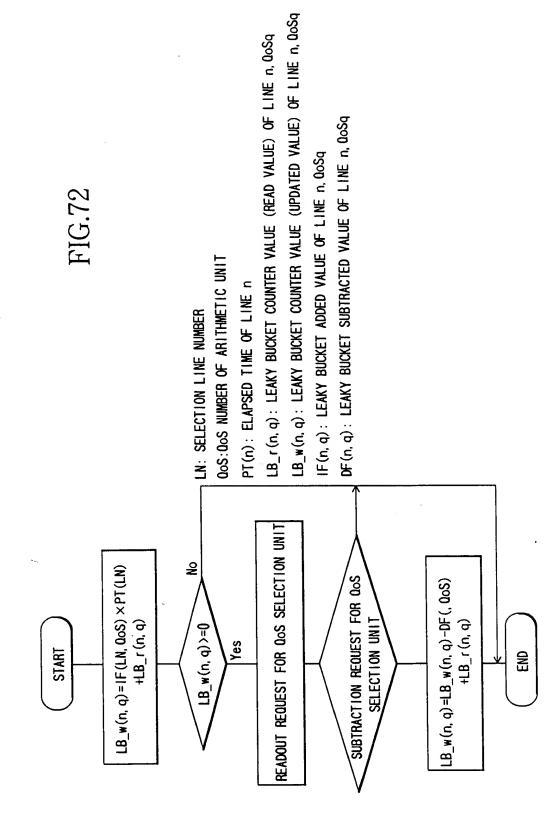


FIG.73

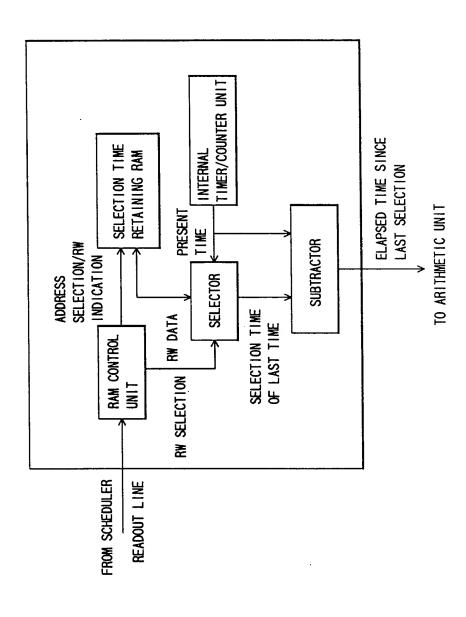


FIG. 74(b) TIME REGION BASED VALID TIME CHECKING METHOD

FIG. 74(a)LAST-TIME SELECTION TIME RETAINING RAM BIT MAP(EXAMPLE) SELECTION TIME (SAME NUMBER OF BITS AS INTERNAL TIM

SELECTION TIME VALID FLAG(1 BIT)

CLEARING TARGET	8	ပ	Q	4	
PRESENT TIME	∢	89	၁	Q	
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TIME	9		,	s /	7
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FIG. 74(c) THRESHOLD VALUE BASED VALID TIME CHECKING METHOD

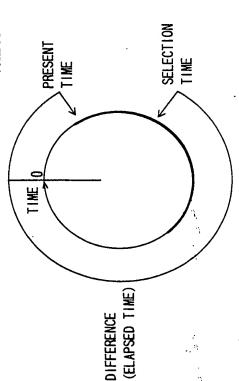
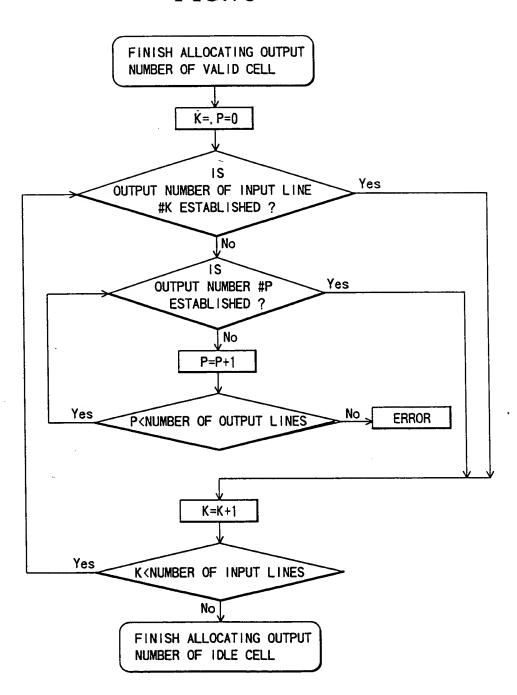


FIG.75



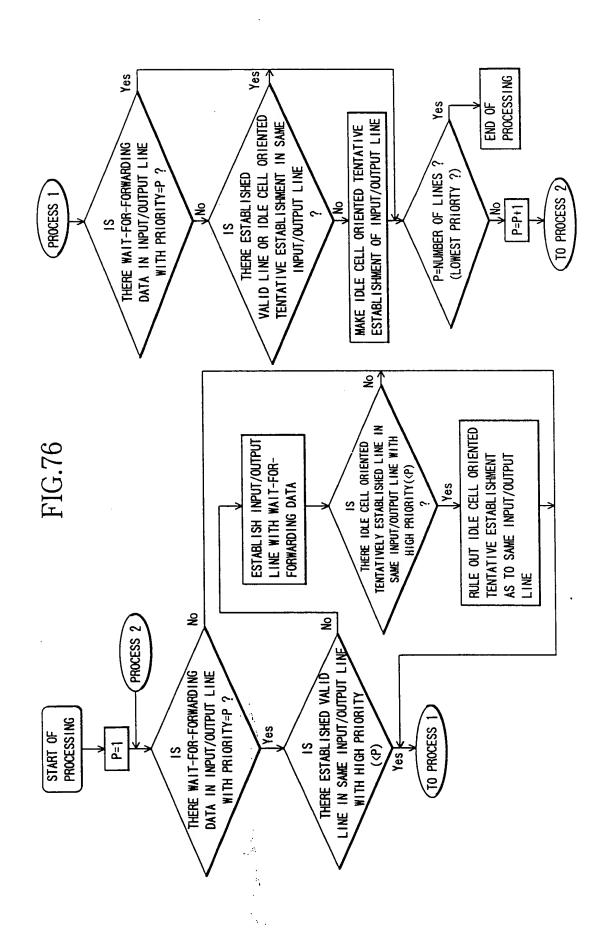




FIG.77

	POINTER=0→	POINTER=1→	POINTER=2→	POINTER=3
INPUT LINE #0	1	4	3	2
INPUT LINE #1	2	1	4	3
INPUT LINE #2	3	2	1	4
INPUT LINE #2	4	3	2	1

FIG.78

·	POINTER=0→	POINTER=1→	POINTER=2→	POINTER=1
INPUT LINE #0	1	4	3	4
INPUT LINE #1	2	1	4	
INPUT LINE #2	3	2	1	2
INPUT LINE #2	4	3	2	3

FIG.79

	1ST	2ND	3RD
INPUT LINE #0	OUTPUT LINE #0	OUTPUT LINE #2	OUTPUT LINE #1
INPUT LINE #1	OUTPUT LINE #2	OUTPUT LINE #1	OUTPUT LINE #0
INPUT LINE #2	OUTPUT LINE #1	OUTPUT LINE #0	OUTPUT LINE #2

FIG.80

	OUTPUT LINE #0	OUTPUT LINE #1	OUTPUT LINE #2
INPUT LINE #0	1	2	3
INPUT LINE #1	3	1	2
INPUT LINE #2	2	3	1